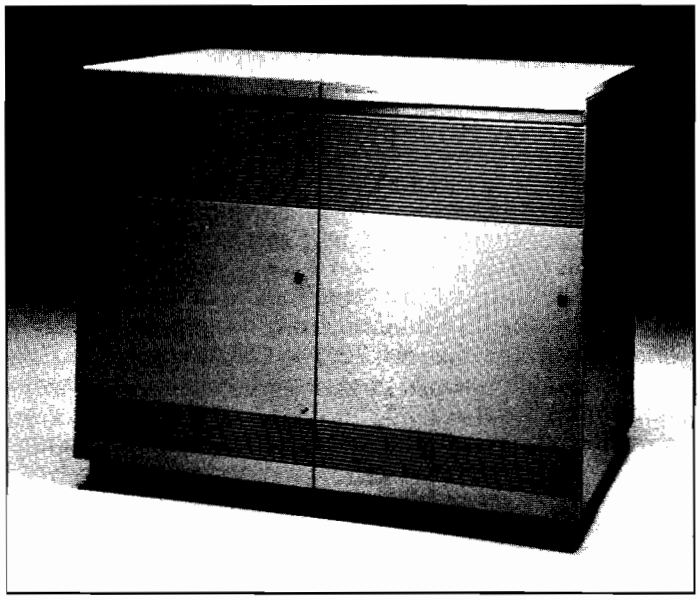
HEWLETT-PACKARD

HP 3000 Computer Systems

Series 930

Product Description

The HP 3000 Series 930 is the first member of the HP 3000 family to utilize the RISC-based HP Precision Architecture. Using the enhanced MPE XL operating system, the Series 930 is an outstanding solution for systems requiring high performance in multi-user, multi-tasking interactive and batch environments. As a new member of the proven HP 3000 family, the Series 930 provides powerful extensions to the highly-regarded networking and data management capabilities for which the HP 3000 systems are known. In addition to enhanced support for database applications, the Series 930 also excels in computationally-intensive EDP environments. Applications software packages are available for the HP 3000 systems to support a wide variety of financial, manufacturing, and office applications. With these capabilities, the Series 930 provides a true high-performance, general purpose business computing solution. It continues the HP 3000 tradition of a broad family of software-compatible, cost-effective business systems.



System Features

- 4.5 MIPS CPU performance
- HP Precision Architecture
- 48-bit virtual addressing
- 128 Kb high-speed CPU cache
- Advanced instruction pipelining techniques
- 32 Mb memory standard, expandable to 96 Mb
- Optional Floating Point Coprocessor
- 4096-entry Translation Lookaside Buffer for virtual-to-physical address translations
- Battery-backup, auto-restart standard
- Dual I/O busses
- Low power and cooling requirements
- Support for up to 400 users
- Terminal connection via IEEE 802.3 standard Local Area Network
- MPE XL operating system
- Network and relational database management systems standard
- AdvanceNet networking solutions

HP Precision Architecture

The Series 930 uses HP Precision Architecture (HPPA) to achieve high performance and reliability at a low cost. HPPA is based on the concept of Reduced Instruction Set Computing (RISC), a design approach which leads to greatly simplified computers that are optimized to provide the highest performance for a given integrated circuit (IC) technology. In addition to offering higher performance, the inherent simplicity of HPPA means lower cost and higher reliability because machines can be implemented with fewer components.

At the core of HPPA is an instruction set containing 140 carefully selected, fixed-format instructions. Because the instruction set is simple, instructions can be hardwired directly in the Central Processing Unit (CPU). This eliminates the need for microcode and the necessity to decode complex instructions. HPPA utilizes a Load/Store design to reduce the number of relatively slow memory

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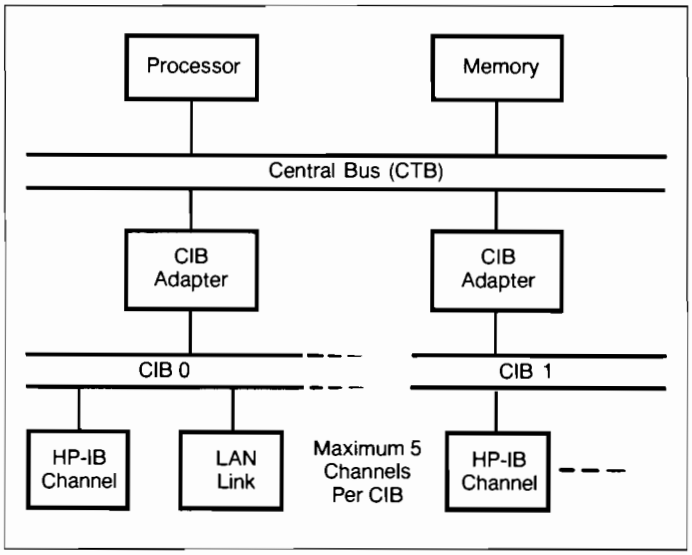
accesses, as most operations are performed register-to-register. To further enhance performance, Optimizing Compilers are used to schedule instructions and manage the instruction pipeline. With hardwired control, a Load/Store design, and Optimizing Compilers, one instruction is executed with virtually every clock cycle. Single cycle execution provides much of the performance benefit of HPPA over traditional architectures.

HPPA also incorporates many other features unrelated to RISC which greatly enhance its functionality. For example:

- Support for coprocessors (i.e. Floating Point)
- Extended addressing
- Memory-mapped I/O subsystem

System Organization

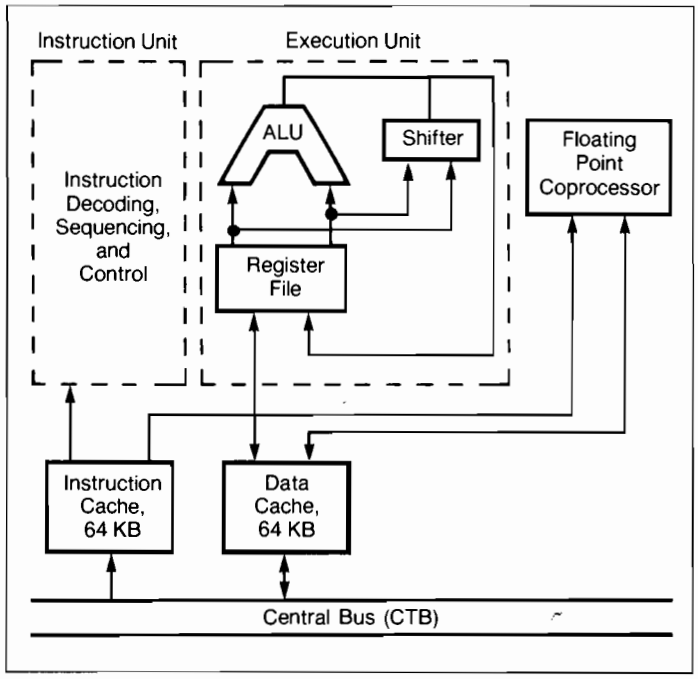
The processor communicates with memory and I/O via the Central Bus (CTB). The Central Bus provides a 32-bit data path, and can support data transfer rates of up to 20 Mb/second. The CTB is interfaced to two separate 16-bit wide Channel I/O Busses (CIBs) via CIB Adapters. The CIBs support I/O interfaces to peripheral devices and datacommunications links.



System Structure

The Series 930 Processor

The Series 930 processor is a five-board set implemented with high-speed Schottky TTL logic. With hardwired control and a three-stage instruction pipeline, the Series 930 is capable of executing one instruction with every 125 nanosecond clock cycle. Separate Instruction and Execution Units facilitate pipelining and allow for efficient, parallel use of processor resources.



Processor Module

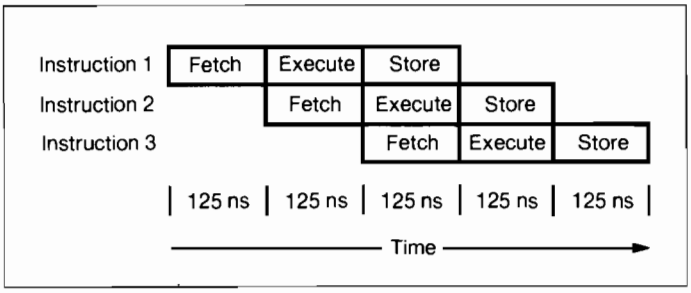
Caches

A total of 128 Kb of high-speed CPU cache is utilized on the Series 930. Utilization of separate instruction and data caches, each 64 Kb, allow the two to operate in parallel, thus increasing processor efficiency and providing higher performance.

Both the instruction cache (I-cache) and the data cache (D-cache) are one-way associative (direct mapped), and are organized as sets of 4096 *cache lines*, with 16-bytes per cache line. The instruction cache is read only, as code is typically assumed to be non-modifiable. A *write-to* cache management scheme is utilized with the data cache. Modified data in the cache is written to main memory only when the processor requires other data to be in that cache location, or when a Direct Memory Access (DMA) operation is performed within that data area, or upon a power fail.

Instruction Pipelining

The Series 930 is pipelined at the instruction level, such that three instructions can be operated on simultaneously. The instruction pipeline consists of three 125 nanosecond stages. During the first stage the instruction is fetched from the I-Cache and decoded. The specified function or calculation is performed during the second stage, and in the third stage the result of the calculation is saved to a CPU general purpose register or cache. Excepting penalties for cache misses, etc., the net effect is that one instruction completes with every 125 ns CPU cycle.



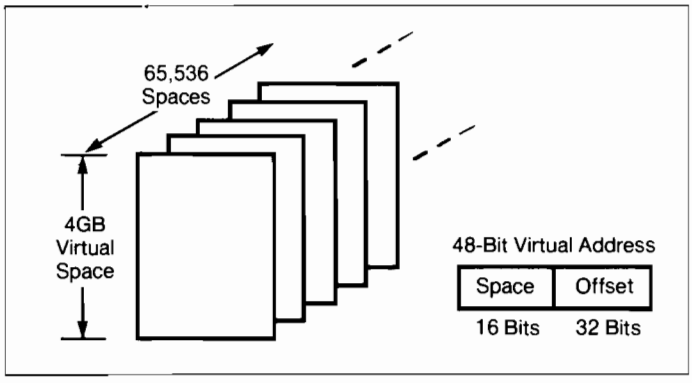
Instruction Pipelining

Floating Point Coprocessor

Single-precision and double-precision floating point calculations can be emulated in software, or performed by an optional Floating Point Coprocessor board. The coprocessor significantly decreases the time required to perform floating point calculations. The Floating Point Coprocessor and the CPU can operate in parallel, thus allowing for increased performance in applications which utilize floating point.

Virtual Memory Management

Virtual Addresses on the Series 930 are 48-bits in length, ensuring sufficient expandability to meet evolving software needs. Virtual Memory is divided into a set of 65,536 *spaces*, with each space 4 Gb in length. Spaces are further divided into fixed length 2 Kb *pages*, with a given page holding either data, code, or both. A single data structure can be up to either 1 Gb or 4 Gb in length (compiler-dependent), and code can span multiple spaces.



Virtual Memory Organization

Virtual Address Translation

Virtual-to-Physical address translation is done by Translation Lookaside Buffers (TLBs), which cache recently accessed virtual page translations, and convert the 48-bit virtual address into a 28-bit physical address. The Series 930 TLB holds translations for 4096 virtual pages, and is split into a 2048-entry instruction TLB and a 2048-entry data TLB. Page-level access protection is provided on the Series 930, and the TLB hardware supports protection mechanisms to ensure that the currently executing process has sufficient authorization to perform the requested data, code, or I/O access.

Memory Subsystem

The Series 930 supports 32 Mb of main memory standard and is expandable to 96 Mb in 8 or 32 Mb increments. The memory subsystem uses 1 M-bit, Nibble-mode Dynamic RAMs. Main memory has battery back up to ensure that information is maintained for a minimum of 15 minutes in the event of an interruption in AC power. This allows the operating system to be automatically restarted and processing to continue without data loss, upon resumption of power.

The internal memory word size is 39 bits, with 32 data bits plus seven bits for error detection and correction. Single-bit memory errors are automatically corrected, with automatic detection of all double-bit errors.

I/O Subsystem

I/O Busses

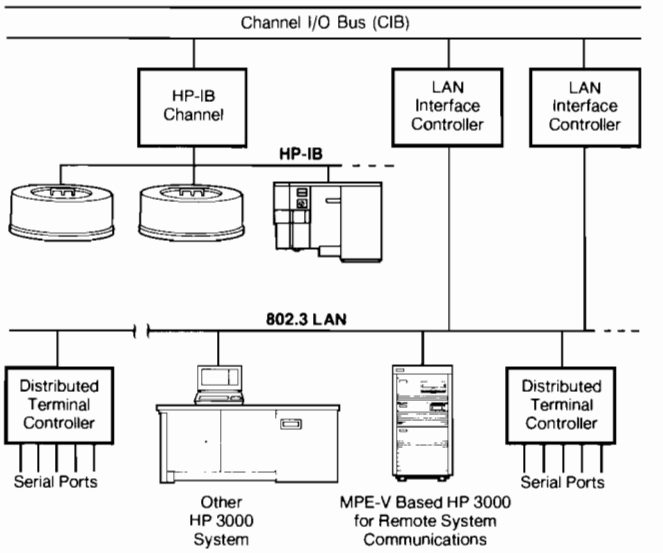
Channel I/O Busses (CIBs) support up to 5 cards each for interfacing peripheral devices and providing datacommunications functions. Each CIB Adapter provides DMA functions and supports up to a 5 Mb/second data throughput capability. The two CIB adapters directly interface with the Central Bus. The CTB runs synchronously with an 8 MHz clock, and can support data transfer rates of up to 20 Mb/second.

Memory Mapped I/O

Input/Output operations are initiated and controlled via a memory-mapped I/O scheme, such that the processor only needs to access reserved virtual or physical memory locations to control I/O operations. Memory Mapped I/O allows for streamlined I/O operations and thus increases system performance in I/O intensive applications.

Peripheral Connections

Discs, tapes, and printers are connected via an HP-IB Channel which supports the 8-bit wide, IEEE-4888 standard Hewlett-Packard Interface Bus (HP-IB). Each HP-IB card supports up to six peripheral devices.



I/O Attachments

Workstation and Serial Printer Connection

Connections for workstations, serial printers, and other serial devices are provided via Distributed Terminal Controllers (DTCs), which are distributed over an IEEE 802.3 standard Local Area Network (LAN). This flexible connection scheme allows DTCs to be situated in the department that they service, saving the cost and effort of running cables from each workstation back to the processor. Each DTC can support up to 48 direct connect ports, or 36 modem ports, or a combination of the two. Both RS-232 and RS-422 interfaces are supported.

System-to-System Datacommunications

AdvanceNet compatible local HP 3000 to HP 3000 communications are supported via the LAN, with available services including Network File Transfer, Remote File Access, Virtual Terminal, and Remote Data Base Access to TurboIMAGE databases.

IBM communications, including SNA NRJE/IMF and Bisync RJE, MRJE, and IMF, as well as remote HP 3000 to HP 3000 communications, are supported via an HP 3000 MPE-V based system acting as a datacomm server on the LAN.

Environmental Specifications

AC Input Voltage (Nominal)
200-240 VAC, Single Phase

Input Voltage Tolerance
±15% (from Nominal)

Input Voltage Frequency
50 Hz −60 Hz (−5%, +10%)

Input Current
13 amps

Input Power Consumption, Max.
2150 watts

Heat Dissipation, Max.
7300 BTU/hour

Physical Dimensions

Height:	1.0 meter (39 Inches)
Width:	1.2 meter (46.8 Inches)
Depth:	0.8 meter (31.2 Inches)

Weight
318 Kg (700 lbs)

Operating Temperature, System
20-25.5 degrees C (68-78 degrees F)

Relative Humidity, System (Operating)
40-60% (non-condensing)

Altitude (Operating)
Up to 15,000 feet

Battery Backup Time, Minimum
15 minutes

Acoustics
66 dB (A) Sound Power

Regulatory Compliance

Safety
UL Listed, CSA Certified
Compliant to IEC 380/435

Electromagnetic Interference
Complies with FCC Rules and Regulations, Part 15, Subpart J, as a Class A computing device. FTZ individual permit (Level A Serial License).

System Software

Listed below are software products currently available for the HP 3000 Series 930. This list will be expanded in the near future as development and testing of additional software products continues.

Operating System
MPE XL

Datacommunications
Network Services (NFT, RFA, VT, RDBA)
HP SNA Server Access/XL
HP AdvanceLink

Utilities
EDIT/V
FCOPY/XL
SORT-MERGE/XL
TDP/V
HP Spell/V

Languages
COBOL II/XL
HP Pascal/XL
HP FORTRAN 77/XL
HP Business BASIC/V
SPL/V
RPG/V

Information Management
ALLBASE/XL
TurboIMAGE/XL
TurboIMAGE DBchange/V
TurboIMAGE Profiler/V
Inform/V
Report/V
HP Toolset/XL
Query/V
Transact/V
VPLUS/V
HP System Dictionary/XL
Dictionary/V
KSAM/V

Application Software

A wide range of manufacturing, financial, and information management applications are available for HP 3000 systems. Your HP Sales Representative can provide further information regarding specific applications on the Series 930.

Supported Peripherals

Listed below are peripheral devices currently available for the HP 3000 Series 930. This list will be expanded in the near future as development and testing of additional peripherals continues.

Terminals

2392A Block-mode terminal, 2397A and 2627A Color Graphics Terminals, 2393A Black and White Graphics Terminal, 2624B Forms Terminal, 2622 Data Entry Terminal. Portable PLUS, VECTRA, and HP 150 Touchscreen Personal Computers supported as workstations. Maximum 400 workstations per system.

Disc Drives

7933H, 7937H Fixed Media and 7935H Removable Media Disc Drives. Maximum 24 discs.

Tape Drives

7974A and 7978A/B half-inch tape drives. Maximum eight per system.

System Printers

2565A 600 LPM and 2566A/B 900 LPM line printers; Maximum eight per system. 2680A and 2688A Page Printers; Maximum four per system.

Serial Printers

2686A Page Printer and 2934A 200 CPS dot matrix printer. Maximum 32 Remote Printers.

Support Services

A wide range of hardware and software support services are available worldwide for all HP 3000 products. Contact your HP Sales Representative for details on available support services.

Ordering Information

The HP 3000 Series 930 SPU includes 32 Mb main memory, two CIBs, one LAN interface, and two HP-IB channels. The SPU hardware is available either without system software, or as part of a preconfigured system. As shown below, the preconfigured system product includes SPU hardware, operating system, data management software, and migration utilities. Return credits are available when upgrading most other HP 3000 systems to the Series 930.

Product Number	Description
32481A	HP 3000 Series 930 SPU Hardware. Includes processor with 32 Mb Memory, two CIBs, two HP-IB Channels, one LAN interface
32480A	HP 3000 Series 930 Preconfigured System. Includes Series 930 SPU, MPE XL Operating System, System Dictionary/XL, ALLBASE/XL Data Management System, TurboIMAGE/XL, QUERY/V, KSAM/V, VPLUS/V, SORT-MERGE/XL, EDIT/V, FCOPY/XL, DEBUG/V, Migration Utilities

Printed in U.S.A. M0587
5954-9439

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