HP 9000 Series 800 Systems
Model 825S
Model 835S/835SE
Model 845S/845SE

Technical Data

HP 9000 Series 800 Midrange Systems

The HP 9000 Models 825S, 835S/835SE, and 845S/845SE provide a highly reliable, cost effective solutions to midrange computing needs. Hewlett-Packard has combined Very Large Scale Integration (VLSI) technology with HP Precision Architecture (HP-PA) to deliver the system processing power needed in a multiuser environment.

The HP 9000 Models 825S, 835S and 845S are well suited for applications requiring midrange performance for relatively small departments. The HP 9000 Models 835SE and 845SE add three additional features as standard: additional I/O ports through the use of an I/O expander, additional memory, and a powerfail recovery system to prevent data loss. These additional features which are available as options or upgrades to the 825S, 835S, or 845S, make these systems suitable for applications requiring a larger number of users.

Like the other Series 800 systems, the HP 9000 Models 825S, 835S/835SE, and 845S/845SE all run the HP-UX operating system,

a superset of AT&T's UNIX® System V Interface Definition (SVID). HP-UX provides an excellent environment for computation, database, graphics, and software development applications requiring a powerful and flexible operating system.

Also, the HP 9000 Models 825S, 835S/835SE, and 845S/845SE all leverage the same packaging. This means that all the systems can be field upgraded to a system offering more compute power and/or additional I/O connectivity in an easy, cost-effective way.

Features

- HP Precision Architecture
- single-chip VLSI central processing unit (CPU)
- advanced instruction pipelining techniques
- real-time clock with battery backup
- 48-bit virtual addressing
- up to two I/O channels with 5-Mbytes/sec each
- support for numerous HP peripherals
- remote access capability for invoking diagnostics and system reset (optional)

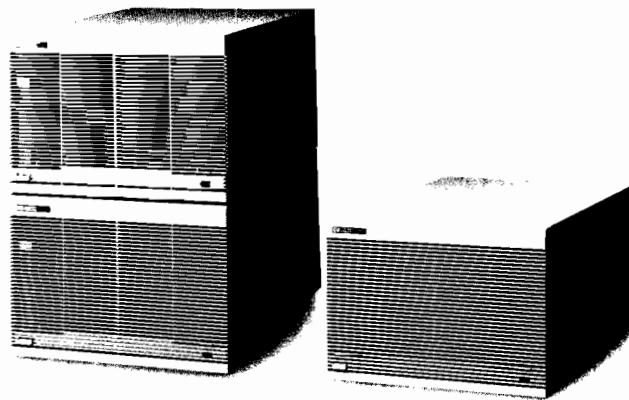**Figure 1. HP 9000 Series 800 Models 825S, 835S/SE and 845S/SE leverage identical packaging**

Table 1. HP 9000 Series 800 mid-range systems at-a-glance

	825S	835S	835SE	845S	845SE
Performance (MIPS)	7	14	14	22	22
Floating point (MFLOPS)*	.54	2.02	2.02	2.50	2.50
Memory	8 – 128 Mbytes	8 – 128 Mbytes	8 – 128 Mbytes	8 – 128 Mbytes	8 – 128 Mbytes
Standard memory	8 Mbytes	8 Mbytes	24 Mbytes	16 Mbytes	32 Mbytes
Maximum I/O bandwidth (sustained)	5 Mbytes/sec	5 Mbytes/sec	10 Mbytes/sec	5 Mbytes/sec	10 Mbytes/sec
Maximum disk storage	21.44 Gbytes	21.44 Gbytes	21.44 Gbytes	21.44 Gbytes	21.44 Gbytes
Cache size	16 Kbytes	128 Kbytes	128 Kbytes	256 Kbytes	256 Kbytes
I.C. technology	NMOS III	NMOS III	NMOS III	NMOS III	NMOS III

*Double precision, coded BLAS

- high performance floating-point coprocessor
- support for 128-Mbyte ECC RAM in 8-, 16-, or 32-Mbyte increments

HP Precision Architecture

The HP 9000 Series 800 computer systems use HP Precision Architecture to provide high performance and reliability at a low cost.

HP-PA is built upon Reduced Instruction Set Computing (RISC), a design approach that delivers greatly simplified computers that are optimized to provide the highest performance for a given integrated circuit technology. The inherent simplicity of HP-PA means machines can be implemented with fewer components to achieve higher reliability.

At the core of HP-PA is an instruction set containing 140 carefully selected, fixed format instructions. Because the instruction set is simplified, instructions can be hardwired directly into the CPU. Hardwiring eliminates microcode and the necessity to decode complex instructions. HP-PA utilizes a load/store design and register-to-register operations to reduce memory access times. To further enhance performance, optimizing compilers

schedule instructions and manage the instruction pipeline. With hardwired control, a load/store design, and optimizing compilers, instructions can be executed on virtually every clock cycle. Single cycle instruction execution accounts for much of the superior performance of HP-PA.
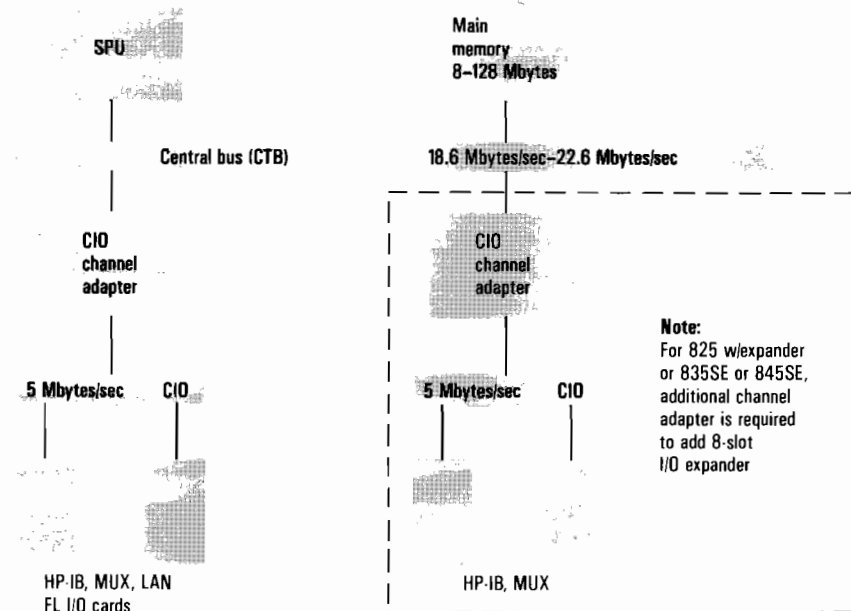
VLSI technology

The HP 9000 Models 825S through 845SE use the powerful design of HP's NMOS III VLSI technology. This technology allows the entire CPU to be integrated onto a single chip. This

technology has allowed the entire processor including the cache, Translation Lookaside Buffer (TLB) and floating-point coprocessor to be implemented on two printed circuit boards for the 825S, and just one printed circuit board for the 835S/835SE and 845S/845SE SPUs. HP's reduced complexity means fewer components and higher reliability to you, all at a lower cost.

System organization

The processor communicates with memory and I/O via the Central Bus (CTB). The CTB pro-

Figure 2. HP 9000 Models 825S, 835S, 835SE, 845S and 845SE system organization

SPU

Central bus (CTB)

CIO channel adapter

5 Mbytes/sec   CIO

HP-IB, MUX, LAN
FL I/O cards

Main memory 8–128 Mbytes

18.6 Mbytes/sec–22.6 Mbytes/sec

CIO channel adapter

5 Mbytes/sec   CIO

HP-IB, MUX

Note:
For 825 w/expander or 835SE or 845SE, additional channel adapter is required to add 8-slot I/O expander

vides a 32-bit wide data path and can support sustained data transfer rates up to 18.6 Mbytes/sec (825S) and 22.8 Mbytes/sec for the 835 and 845 systems. The Central I/O Bus interfaces with the Channel I/O Bus via the Channel Adapter. The Channel I/O Bus supports sustained I/O data transfer rates of 5-Mbytes/sec and supports interfaces to peripheral devices and data communications links.

Processors

The HP 9000 Model 825S processor is contained entirely on two boards utilizing HP's proprietary NMOS III VLSI technology. The main processor board consists of six VLSI chips, including the Central Processing Unit (CPU), a Translation Lookaside Buffer control unit (TCU), two Cache Control Units (CCUs), a System Interface Unit (SIU), and a Math Interface Unit (MIU). The second board is called the system board and contains the floating-point coprocessor and the Channel I/O Adapter.

The HP 9000 Models 835S/835SE and 845S/845SE processors reside entirely on one printed circuit board. The processor board contains eight VLSI chips: the CPU, the TCU, two CCUs, a floating-point controller (FPC), and an SIU. The processor board also contains two commercially available VLSI floating-point math chips (ALU and Multiplier). The Channel I/O Adapter and real-time clock reside on a second board, the Processor Dependent Hardware (PDH) board. In the 835SE and 845SE, the PDH also contains a second Channel I/O Adapter which connects to the I/O expander. The real-time clock

has a battery backup to maintain time and date while the system is powered down.

Cache

The use of a cache enhances system performance by minimizing CPU requests for instructions or data stored in memory. By storing frequently used instructions and/or data in a high-speed cache memory, the CPU can execute instructions or process data without using the SIU and the CTB.

The cache operates in a write-back mode. Write-back means that the cache writes modified data to system memory only when the processor needs the cache location for other data, when the operating system flushes the cache location due to a Direct Memory Access (DMA) operation, or in the event of a power failure. This efficient

cache operation provides maximum system throughput. Parity checking protects the cache, and a parity error triggers a recovery algorithm that resolves most failures.

The HP 9000 Models 825S, 835S/835SE, and 845S/845SE all use a two-set associative, high-speed cache. The Model 825S has a total of 16-Kbytes of high-speed CPU cache memory. Models 835S and 835SE utilize a 128-Kbyte cache while Models 845S and 845SE utilize a 256-Kbyte cache.

Instruction pipelining

Models 825S, 835S/835SE, and 845S/845SE all utilize staged instruction pipelining that allows operations on multiple instructions simultaneously. The net effect is that one instruction completes with essentially every instruction clock cycle. The 825S,

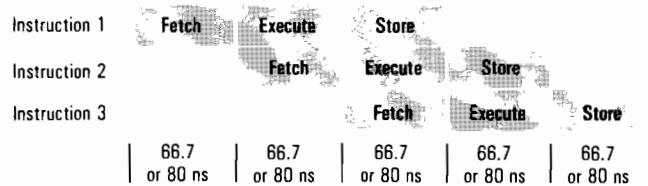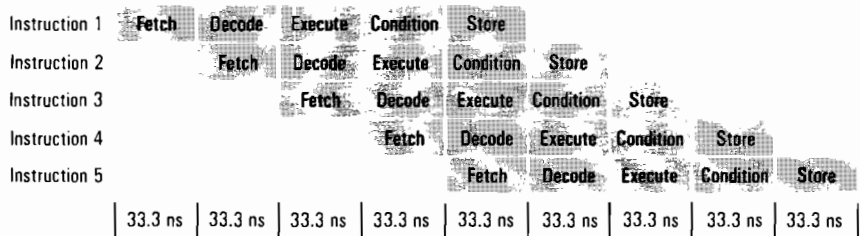**Figure 3. Models 825S, 835S and 835SE pipelining diagram**

Figure 4. Models 845S and 845SE pipelining diagram

835S, and 835SE all utilize a three-stage pipeline. Models 845S and 845SE utilize a five-stage pipeline. For the 825S, the instruction cycle time is 80 nanoseconds. For Models 835S and 835SE the instruction cycle time is 66.7 nanoseconds. The instruction cycle time for the 845S and 845SE is 33.3 nanoseconds.

Floating-point coprocessor

Single- and double-precision floating-point calculations are performed by the floating-point coprocessor. The coprocessor significantly decreases the time required to perform floating-point calculations. The floating-point control unit allows floating-point operations to overlap with CPU operations, as long as there is no interlocking data. This ability to operate in parallel allows for increased performance in applications which are computation-intensive.

Virtual memory

Virtual addresses are 48-bits in length, ensuring ample expandability to meet growing software needs. Virtual memory is divided

Figure 5. Virtual memory organization

65,535 space

4 Gbytes virtual space

48-bit virtual address

Space **Offset**

16 bits 32 bits

into 65,535 spaces with each space 4 Gbytes in length. Spaces are further divided into fixed-length 2-Kbyte pages, with a page holding code or data. A single data structure can be up to 1 Gbyte in length. The virtual memory scheme can accommodate memory of more than 260,000-Gbytes.

The Translation Lookaside Buffer (TLB) performs translations from virtual addresses to physical addresses. The TLB stores recently accessed virtual page translations and converts the 48-bit virtual address into a 29-bit physical address. The TLB for the 825S holds translations for 2048 virtual pages, the 835S and 835SE holds translations for 4096 virtual pages, and the 845S and 845SE hold translations for 16,384 virtual pages. This is enough room to map 4-, 8-, and 32-Mbytes of system memory, respectively. The memory for the virtual pages is split into two parts, half for an instruction TLB and half for a data TLB. This split allows parallel translation of instruction and data addresses.

All five systems provide page-level access protection. The TLB hardware supports protection mechanisms to ensure the cur-

rently executing process has sufficient authorization to perform the requested data, code, or I/O access. The TLB also uses parity checking which signals the CPU when errors are found.

Memory subsystem

Models 825S and 835S include 8-Mbytes of Error Checking and Correcting (ECC) memory. Models 845S, 835SE and 845SE include 16-, 24-, and 32-Mbytes of ECC memory, respectively. The ECC memory is expandable in 8-, 16-, and 32-Mbyte increments to 128-Mbytes. The 8-Mbyte and 16-Mbyte memory boards use 1-Mbit Nibble-mode dynamic RAMS, while the 32-Mbyte board utilizes 4-Mbit dynamic RAMS.

The internal memory word size is 72 bits, with 64 bits for data and 8 bits for error detection and correction. Rare double-bit errors are automatically detected, causing an interrupt or a high-priority machine check. Single-bit errors are automatically corrected. The ECC memory assures high memory performance and availability. The powerfail battery backup (optional on the Model 825S, 835S, and 845S; standard on the Model 835SE and 845SE) protects the system from AC power loss such that if power is lost, the state of the processor is stored in memory for at least 15 minutes. Maximum storage time depends on the amount of memory in the system. If power is restored within this limit, the system restores itself and resumes processing.
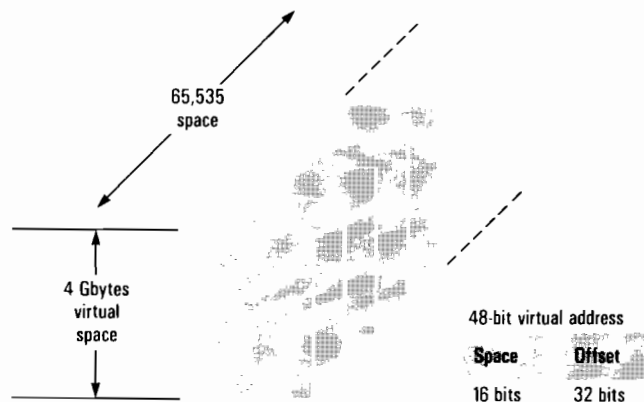
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I/O subsystem

Channel I/O bus

All system models use a 16-bit, 5-Mbyte/sec bandwidth (sustained) channel I/O bus to connect peripheral and data communication cards. The channel I/O bus has seven I/O slots for the 825S and 835S, and six I/O slots for the 845S. Two slots contain the HP-IB card and the 6-channel Multiplexer interfaces shipped with each system. Models 835SE and 845SE come with a second channel I/O adapter and an I/O expander (I/O expander can be ordered as an option to the 825S) that provide eight additional I/O slots (seven for the 825S).

Channel I/O adapter

Channel I/O adapters manage I/O by interfacing the central bus with the channel I/O bus, synchronizing the different speeds and bandwidths. Channel I/O adapters also manage Direct Memory Access (DMA) transfers between system memory and channel I/O interfaces with their associated peripherals. The channel I/O adapter accomplishes this function with little CPU intervention, interrupting only to signal completion of DMA transfers. Large blocks of data can be transferred to and from system memory at rates of up to 5-Mbytes per second (sustained) per channel with negligible CPU overhead.

**Figure 6. Model 825S with I/O expander**
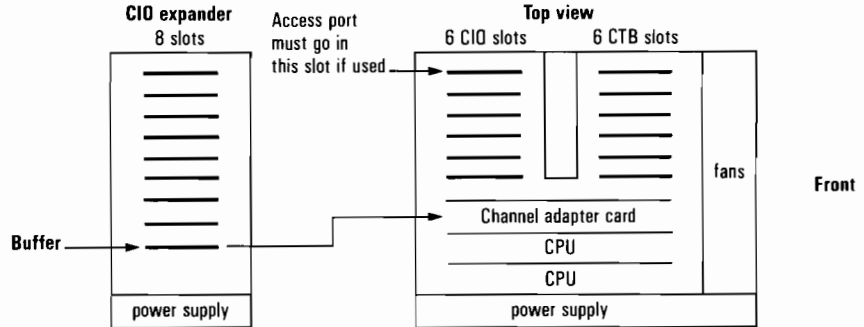
- 825S comes standard with one 6-channel MUX, one HP-IB and 8-Mbyte ECC RAM
- Additional channel adapter card uses one CIO and one CTB slot
- 825S without expander has seven CIO and seven CTB slots available

Figure 7. Model 835S/SE backplane physical layout
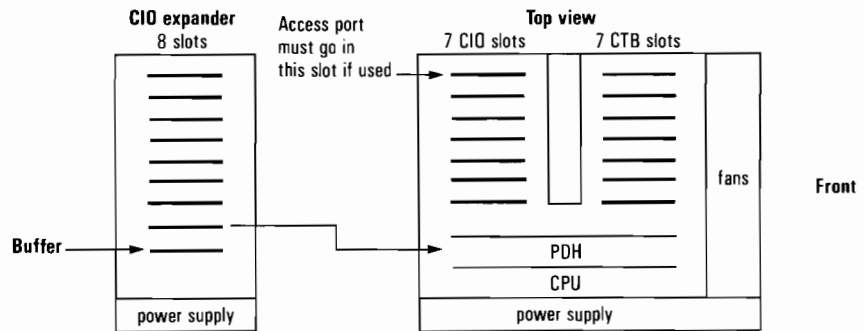
- 835S comes standard with one 6-channel MUX, one HP-IB, 8-Mbyte ECC RAM
- 835SE comes standard with one 6-channel MUX, one HP-IB, 24-Mbyte ECC RAM, BBU, I/O expander
- I/O expander supported on 835SE only

Figure 8. Model 845S/SE backplane physical layout
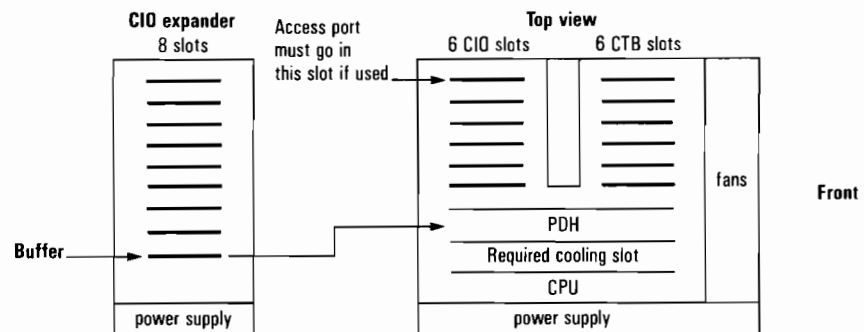
- 845S comes standard with one 6-channel MUX, one HP-IB, 16-Mbyte ECC RAM
- 845SE comes standard with one 6-channel MUX, one HP-IB, 32-Mbyte ECC RAM, battery back-up unit, 8-slot I/O expander
- I/O expander supported on 845SE only

Peripheral connections

Disk drives, tape drives, printers, and plotters connect to Models 825S, 835S, 835SE, 845S, and 845SE via an HP-IB card that supports the 8-bit wide, IEEE 488 standard. Each HP-IB card interfaces with up to four high-speed devices or 14 low-speed devices.

Certain disk drives can be connected via the HP-FL card, which is a fiber-optic link card. Each HP-FL channel can support eight disk drives at up to 5-Mbytes per second per channel.

Six-channel multiplexers are available to connect workstations, terminals, modems, serial printers, and other serial devices. Local Area Network (LAN) interfaces allow connections to other systems, as well as support for distributed terminal controllers (DTCs). DTCs are available to connect serial devices to the system. DTCs are distributed over an IEEE 802.3 standard local area network (LAN), can support up to 48 directly-connected ports, or 36 modem ports, or a combination of the two. Both RS-232 and RS-422 interfaces are supported.

System software features

All HP 9000 Series 800 and Series 600 computers are based on the standards-based multiuser, multi-tasking HP-UX. HP-UX provides object code compatibility among these computers and source code compatibility with Series 300 computer systems. The operating system is based on AT&T's UNIX® System V Release 3.0, and passes AT&T's System V Interface Definition (SVID 2). It also incorporates selected features from UC Berkeley Software Distribution 4.3 (BSD). In addition, HP-UX conforms to the *X/OPEN™ Portability Guide Issue 2 (XPG2), the IEEE's POSIX 1003.1, and the Federal Processing Specification (FIPS) 151-1. Compliance with these standards facilitates portability of applications developed on other standards-based operating systems.

HP-UX meets the growing needs for highly available, powerful systems by supporting a disk mirroring product** for environments where no data can afford to be lost due to disk failures. In addition, HP-UX supports a diskless computing environment, which significantly reduces the cost and increases the information shared by different users over the LAN. HP's standards-based operating system also contains features

intended to fulfill the Department of Defense C2 Trusted Systems Requirements. And finally, HP-UX supports all the popular languages in the computing world and a rich assortment of tools for Computer-Aided Software Engineering (CASE), Networking Database Management, and Graphics. For detailed information on the HP-UX operating system, please see the HP-UX Technical Data sheet.

Application software

Over 1000 application software packages are available for the HP 9000 Series 800 and Series 600 systems. Contact your HP sales representative for information regarding specific applications.

**Not available on HP 9000 Models 808S, 815S, and 832S.

Supported peripherals

The following list contains peripherals supported by the HP 9000 Models 825S, 835S/835SE, and 845S/845SE systems at the time of this publication. The list of supported peripherals changes as new peripherals are introduced and other peripherals are discontinued. Contact your local HP sales representative for more information on currently supported peripherals.

Support services

A wide range of hardware and software support services are available worldwide for HP 9000 products. Contact your HP sales representative for details on available support services.

Warranty information

The warranty covering your specific system is determined by the HP Warranty and Installation Terms in effect at the time of purchase. Contact your HP sales representative for a copy.

Table 2. Peripherals supported on HP 9000 Series 800 mid-range systems

Terminals	Disk drives	Tape drives	Printers
HP C1001A/G/W	HP 7936H	HP 7979A	HP 2225D
HP C1002A/G/W	HP 7936FL	– Opt. 800	HP 2227A
HP C1003A/G	HP 7937H	HP 7980A	HP 2228A
HP C1004A/G/W	HP 7937FL	– Opt. 800	HP 2276A
HP C1006A/G/W	HP 7957B	HP 7980XC	HP 2277A
HP C1007A/G/W	HP 7958B	HP 9144A	HP 25638
HP 2393A	HP 7959B	HP 9145A	HP 2564B
HP 2397A	HP 7962B	HP 35401A	HP 2566B
HP 3082B	HP 7963B		HP 2567B
HP 9666A	HP 9122C		HP 2684A/D/P
	HP 9127A		HP 2934A
	HP 9153C Opt. 040		HP 33440A
	HP 9292B		HP 33447A
	HP 9263B		HP 3630A
	HP 97902B		HP C1602A
	HP 97903B		
	HP 97962B		
	HP 979638		
	HP 50710A		
	HP C2200A		
	HP C2201A		
	HP C2203A		
	HP C2204A		

Table 3. SPU technical specifications

Electrical specifications

(Models 825S, 835S, 835SE, 845S, 845SE)	Line voltage	Voltage tolerance	Line frequency	Maximum current
	100 V	90-110 VAC	48-66 Hz	9.5 A
	120 V	108-132 VAC	48-66 Hz	8.0 A
	240 V	180-264 VAC	48-66 Hz	5.3 A
Power consumption	600 W, 2034 BTU/hr			

Environmental specifications

Temperature	Operating: 0° to +55°C (Models 825S, 835S/SE, 845S/SE)
	Non-operating: –40° to +70°C (Models 825S, 835S/SE, 845S/SE)
Relative humidity	15% to 95% at 40°C, non-condensing (Models 825S, 835S/SE, 845S/SE)
Maximum altitude	Operating: 4,570 m (15,000 ft) (Models 825S, 835S/SE, 845S/SE)
	Non-operating: 15,240 m (50,000 ft) (Models 825S, 835S/SE, 845S/SE)

Regulatory compliance

Electromagnetic interference	Manufacturer's declaration verifies VDE Level B; complies with FCC Rules and Regulation, part 15, subpart J, as Class A computing product; registered as a VCCI Class 1 product
Safety	UL listed (UL 478.5); CSA certified (C22.2 no. 22-M1986); complies with IEC 380 and IEC 435

Physical characteristics

Dimensions	Height: 234mm (9.21 in) (Models 825S, 835S, 845S)
	Height: 468mm (18.43 in) (Models 835SE, 845SE)
	Width: 325mm (12.8 in) (Models 825, 835S/SE, 845S/SE)
	Depth: 500mm (19.7 in) (Models 825S, 835S, 835SE, 845S/SE)
Weight	23 kg (51 lbs) (Models 825S, 835S, 845S)
	39 kg (86 lbs) (835SE, 845SE)
Vibration and shock	HP 9000 Series 800 computer systems are type-tested for normal shipping and handling vibration. Contact your HP sales representative for review of any application requiring operation under continuous vibration.
Acoustics	5.0 Bels (A) Sound Power
Ventilation	Forced air cooling, air flows from front to back

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For more information, call your local HP sales office listed in your telephone directory or an HP regional office listed below for the location of your nearest sales office.

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Monte Pelvoux No. 111
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Melbourne, Australia
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